1. **ECE 4500 Digital Electronics**

2. Credit Hours: 4 hours (3 – 3)

3. Coordinator: Dr. Janos L. Grantner, Professor of Electrical and Computer Engineering
   Instructor in the Fall 2015 Semester: Dr. Janos L. Grantner

4. Textbook(s) and/or Required Materials:
   a. Jan M. Rabaey, *Digital Integrated Circuits*, Second Edition, Prentice-Hall, 2003, ISBN: 0-13-597444-5
   b. Materials disseminated using the ECE 4500 Class Web Page (the official media for the class)

   Recommended Materials:
   a. Instructor's Lecture Notes, available on the ECE 4500 Class Web Page
   b. Richard C. Jaeger, *Microelectronic Circuit Design*, McGraw-Hill, 1997, ISBN: 0-07-032-482-4

   References:
   a. Tutorials on how to use the Mentor Graphics' IC Nanometer Technology tools, available on the ECE 4500 Class Web Page

5. Course information:
   a. 2016-17 Catalog: The electrical and logic aspects of digital integrated circuits and their applications. Transistor-level design and simulation of digital electronic circuits.
   b. Prerequisites: ECE 2210, ECE 2500 and ECE 3570; with a grade of "C" or better in all prerequisites.
   c. Prerequisites by topic:
      1. Electrical circuits
      1. Introductory level digital logic design
      2. Introductory knowledge of computer architecture
   d. Required course in the Computer Engineering program

6. Course Objectives: (ABET Learning Outcomes)
   1. To provide experience to model, analyze, design and simulate digital integrated circuits (a, b, c, e).
   2. To provide experience to work with Mentor Graphics IC Flow tools (k).
   3. To provide experience to choose a suitable circuit design style to meet the required specs (c).
   4. To develop skills to prepare effective written technical communications for engineering analysis and design work through project reports (g).
   5. To assess the students' knowledge of contemporary issues (j).
   6. To assess the students' skills to use modern tools of engineering practice (k).

7. Topics:
   a. Course overview, the state-of-the-art of microelectronics design and nanotechnology
   b. MOSFET transistor models, static and dynamic behavior
   c. The static CMOS inverter: static and dynamic behavior, power consumption, the effects

of technology scaling

d. Design of combinational logic gates in CMOS: static and dynamic design styles, power consumption
e. Design of sequential logic circuits: static and dynamic sequential circuits, non-bistable sequential circuits
f. Design of memory and array structures: the memory core, memory peripheral circuits
g. Timing issues in digital circuits
h. Coping with interconnect

8. Design Projects:
   a. Design of 4-bit parallel ALU (a bonus project is also offered). A report is required.
   b. Design of a Dual 4x4 Bit Register Bank (a bonus project is also offered). A report is required.

9. Laboratory: 9 laboratory experiments

10. Evaluation:
    a. Examinations (50%)
    b. Design projects (20%)
    c. Laboratory(20%)
    d. Homework (10%)

11. Contribution to Professional Component:
ABET professional component content as estimated by faculty member who prepared this course description:
Engineering sciences: 2 credits or 50%
Engineering design: 2 credits or 50%

Prepared by: Dr. Janos L. Grantner

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